

Jun. 2005



SERVICE MANUAL ADDENDUM

IC-F24 IC-F24S IC-F25 IC-F25S

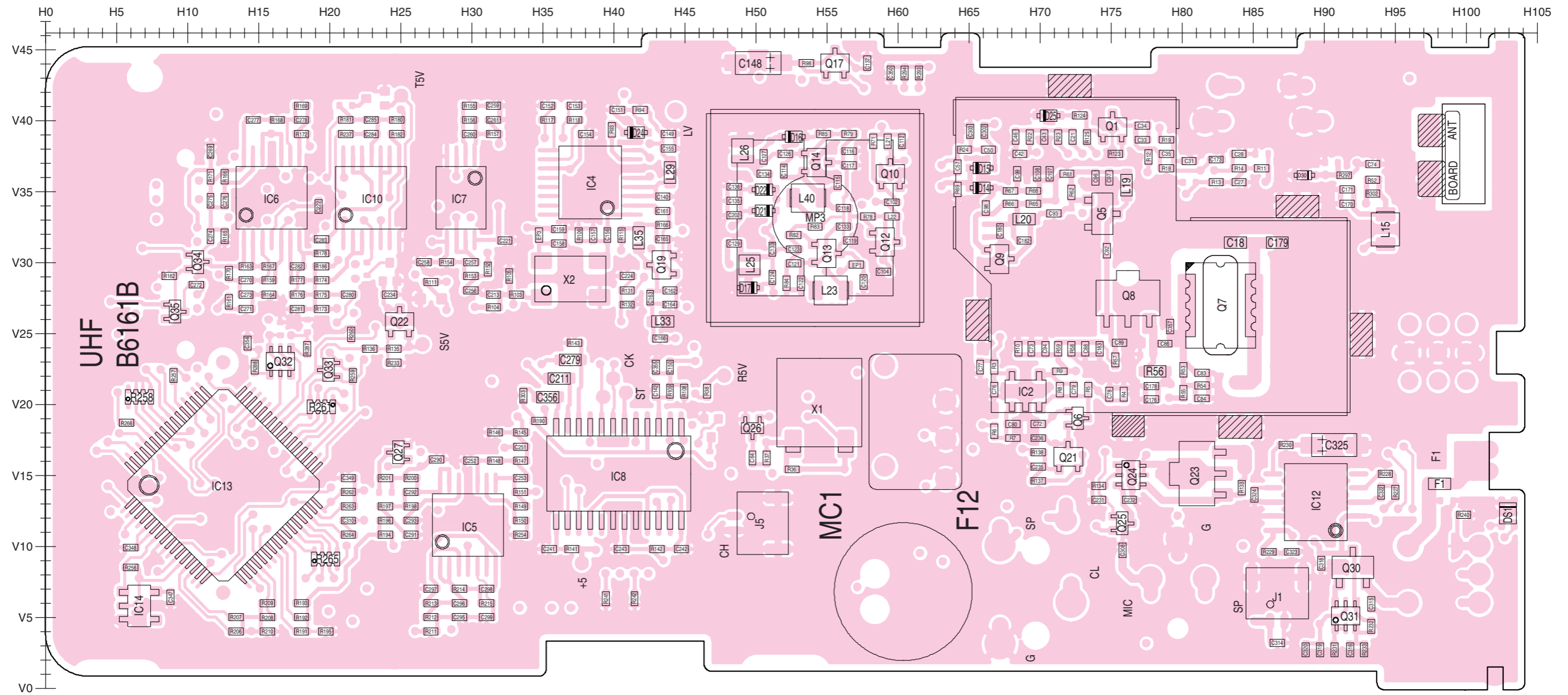
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BOARD LAYOUTS

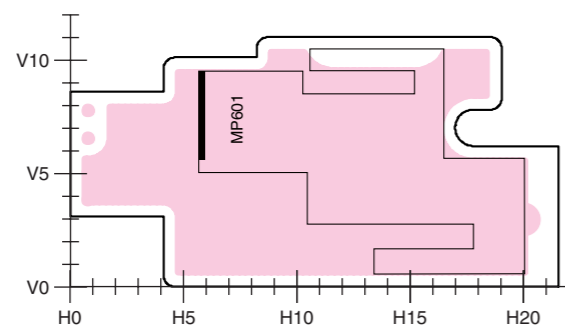
MAIN UNIT

● TOP VIEW



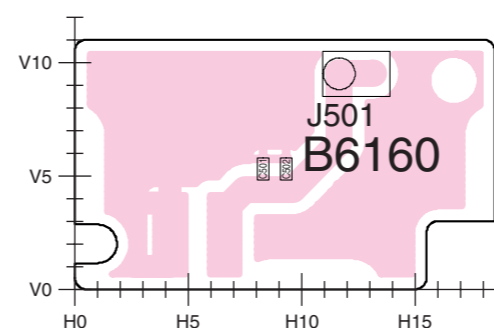
ANT UNIT

● TOP VIEW

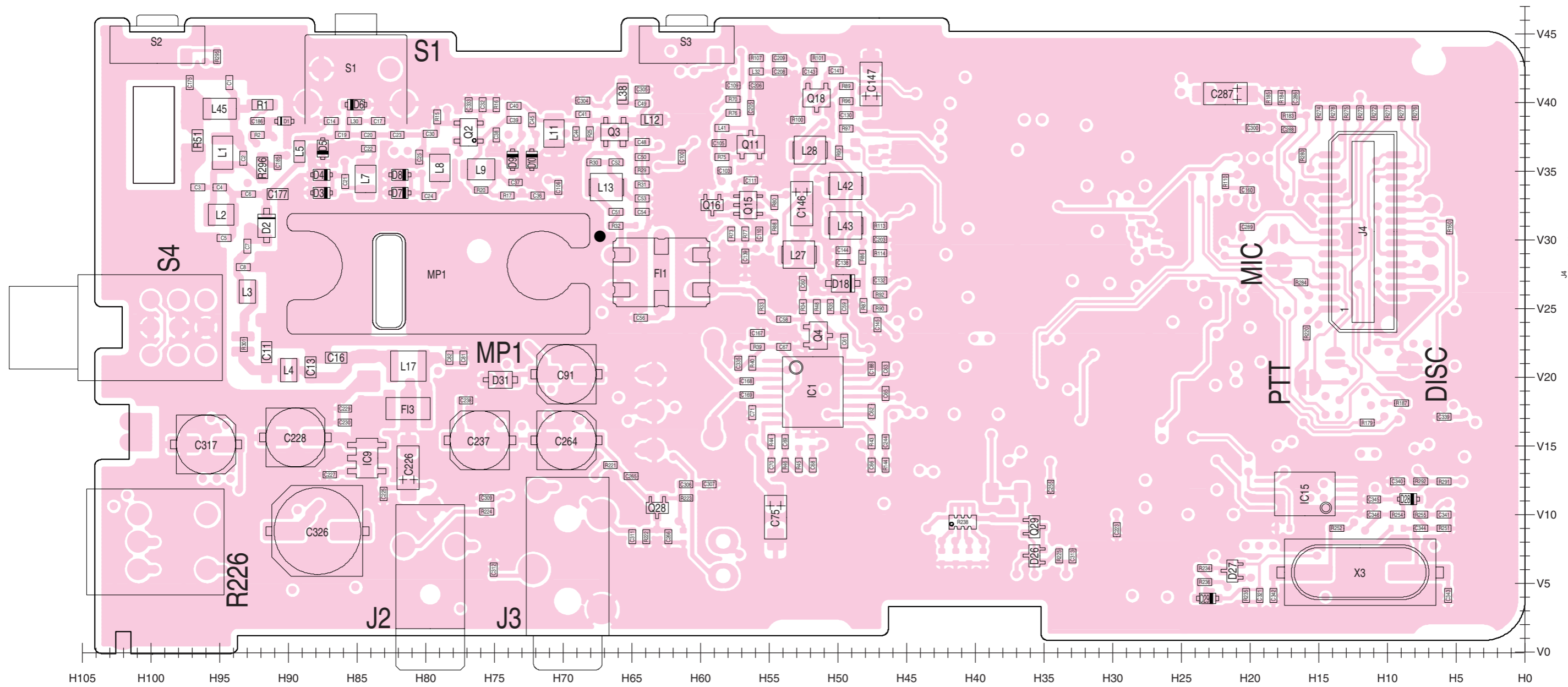


CONNECT UNIT

● TOP VIEW



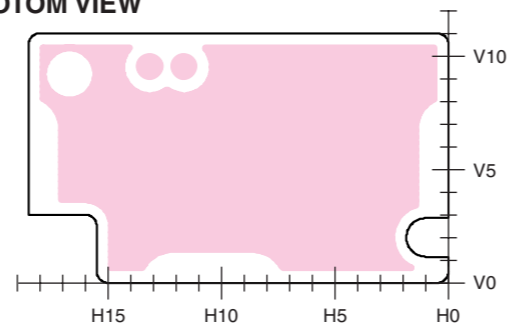
● BOTTOM VIEW



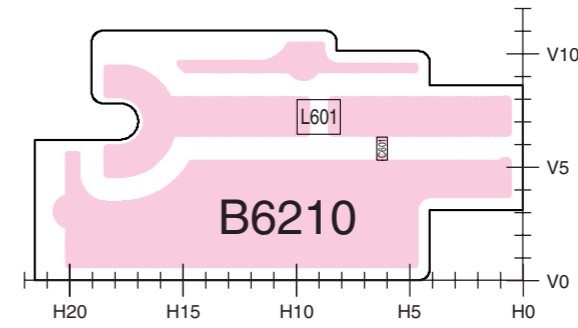
J4 to the OPTIONAL unit

OPV1	SCK
OPV2	SI
DAKT	SO
GND	CRO
OPT3	CCS
OPT2	CP10
OPT1	DISC
SICO	DET
NMI	CP11
BUSY	BEEPO
RES	AFONO
MCIN	CP12
MCOT	VCC
PTT	+5V
PTTI	GND

● BOTOM VIEW

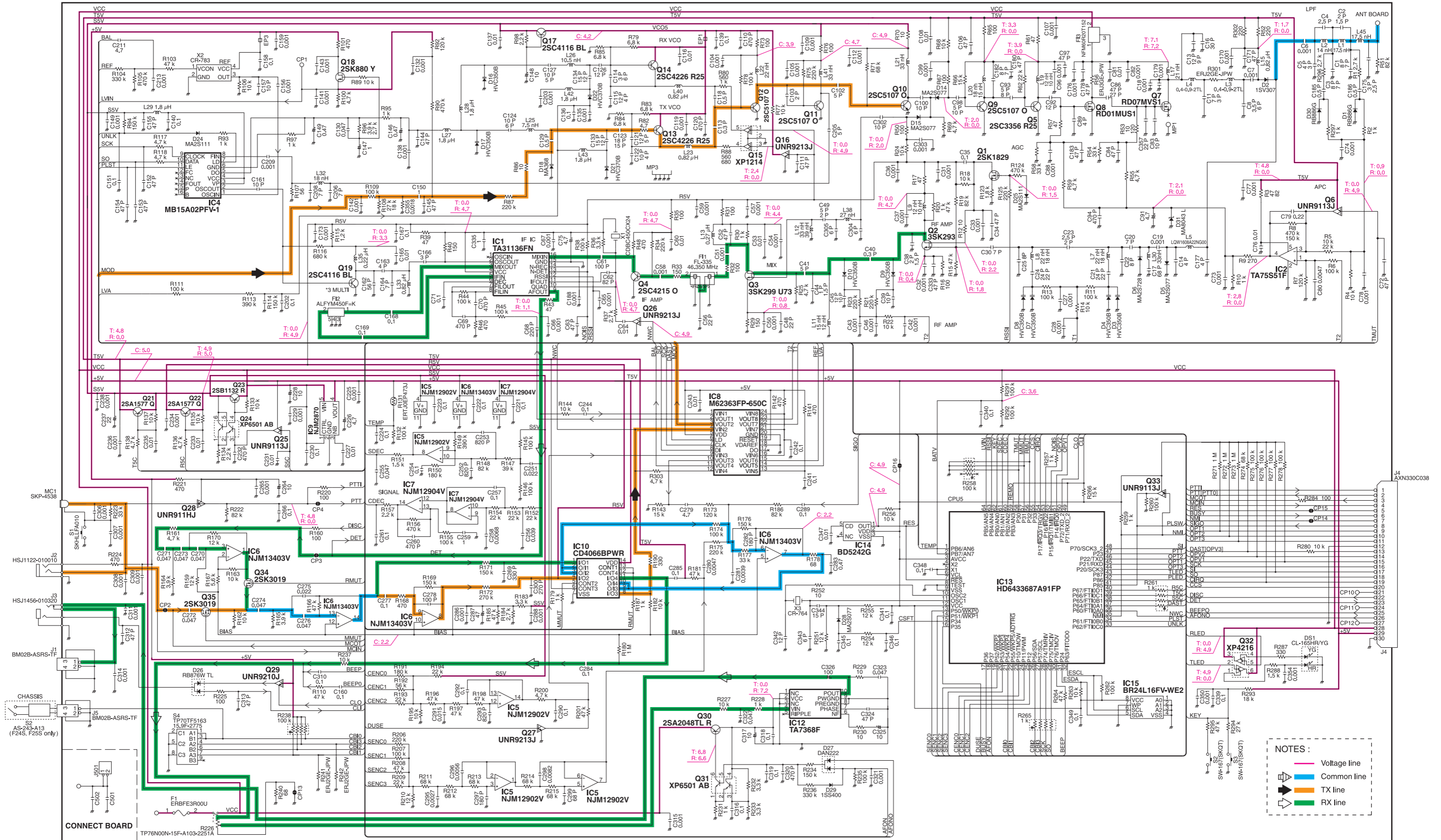


● BOTOM VIEW



VOLTAGE DIAGRAM

MAIN UNIT



- NOTES :
- Voltage line
 - Common line
 - TX line
 - RX line



SERVICE MANUAL

UHF TRANSCEIVERS

IC-F24
IC-F24S
IC-F25
IC-F25S

S-14116IZ-C1-①
Jun. 2005

Icom Inc.

INTRODUCTION

This service manual describes the latest service information for the **IC-F24/IC-F24S/IC-F25/IC-F25S** UHF TRANSCEIVER at the time of publication.

MODEL	VERSION	SYMBOL	CH	FREQUENCY
IC-F24	USA-02	US2	16	400-470 MHz
	USA-03	US3	16	450-512 MHz
	GEN-02	GE2	16	450-470 MHz
	GEN-03	GE3	16	450-520 MHz
IC-F24S	USA-02	US2S	2	400-470 MHz
	USA-03	US3S	2	450-512 MHz
	GEN-02	GE2	2	400-470 MHz
	GEN-03	GE3	2	450-520 MHz
IC-F25	EUR-02	EU2	16	400-470 MHz
IC-F25S	EUR-02	EU2S	2	400-470 MHz

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 8 V. Such a connection could cause a fire or electric hazard.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

2260002840 Switch SKHLLFA010 IC-F24 Main unit 5 pieces
8930063350 Lens 2775 Lens IC-F24 Chassis 10 pieces

Addresses are provided on the inside back cover for your convenience.

REPAIR NOTES

1. Make sure the problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 30 dB to 40 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.


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SECTION 1

SPECIFICATIONS

■ GENERAL

- Frequency coverage : 400–470 MHz [USA-02], [GEN-02], [EUR]
450–512 MHz [USA-03]
450–520 MHz [GEN-03]
- Type of emission :

VERSION	WIDE	MIDDLE	NARROW
[USA], [GEN]	16K0F3E (25.0 kHz)	N/A	11K0F3E (12.5 kHz)
[EUR]		14K0F3E (20.0 kHz)	8K50F3E (12.5 kHz)
- Number of conventional channels : 2 ch (IC-F24S/F25S), 16 ch (IC-F24/F25)
- Antenna impedance : 50 Ω (nominal)
- Operating temperature range : –30°C to +60°C (–22°F to +140°F) [USA], [GEN]
–25°C to +55°C [EUR]
- Power supply requirement : 7.2 V DC nominal (negative ground)
- Current drain (at 7.2 V DC ; approx.) :

RECEIVING		TRANSMITTING	
Stand-by	Max. audio	High (at 4 W)	Low (at 1 W)
75 mA	300 mA	1.6 A	0.8 A
- Dimensions (projections not included) : 53(W)×120(H)×38(D) mm; 2³/₃₂(W)×4²³/₃₂(H)×1¹/₂(D) in
- Weight (Including BP-231) : Approximately 260 g (9³/₁₆ oz)

■ TRANSMITTER

- Output power (at 7.2 V DC) : 4 W
- Modulation : Variable reactance frequency modulation
- Maximum permissible deviation : ±5.0 kHz (Wide), ±4.0 kHz (Middle), ±2.5 kHz (Narrow)
- Frequency error : ±2.5 ppm
- Spurious emissions : 70 dB (min.) [USA], [GEN]
0.25 μW (≤1 GHz), 1.0 μW (>1 GHz) [EUR]
- Adjacent channel power : 70 dB min. (75 dB typical) for Wide
70 dB min. (73 dB typical) for Middle
60 dB min. (68 dB typical) for Narrow
- Audio harmonic distortion : 3% typical (1 kHz, 40% deviation)
- Hum and Noise ([USA], [GEN]) (without CCITT filter) : 40 dB min. (46 dB typical) for Wide
34 dB min. (40 dB typical) for Narrow
- Residual modulation ([EUR] only) (with CCITT filter) : 45 dB min. (55 dB typical) for Wide
43 dB min. (53 dB typical) for Middle
40 dB min. (50 dB typical) for Narrow
- Limiting charact of modulator : 60–100% of maximum deviation
- Microphone impedance : 2.2 kΩ

■ RECEIVER

- Receive system : Double conversion superheterodyne system
- Intermediate frequencies : 1st IF: 46.35 MHz, 2nd IF: 450 kHz
- Sensitivity : 0.25 μV (–119 dBm) typical at 12 dB SINAD [USA], [GEN]
–4 dBμV (–111 dBm) emf typical at 20 dB SINAD [EUR]
- Squelch sensitivity (at threshold) : 0.25 μV typical [USA], [GEN]
–4 dBμV emf typical [EUR]
- Adjacent channel selectivity : 70 dB min. (75 dB typical) for Wide
70 dB min. (73 dB typical) for Middle
60 dB min. (65 dB typical) for Narrow
- Spurious response : 70 dB min.
- Intermodulation rejection ratio : 70 dB min. (74 dB typical) [USA], [GEN]
65 dB min. (67 dB typical) [EUR]
- Hum and Noise ([USA], [GEN] only) (without CCITT filter) : 40 dB min. (45 dB typical) for Wide
34 dB min. (40 dB typical) for Narrow
- Hum and Noise ([EUR] only) (with CCITT filter) : 45 dB min. (55 dB typical) for Wide
43 dB min. (53 dB typical) for Middle
40 dB min. (50 dB typical) for Narrow
- Audio output power : 0.5 W typical at 5% distortion with an 8 Ω load
- Output impedance (Audio) : 8 Ω

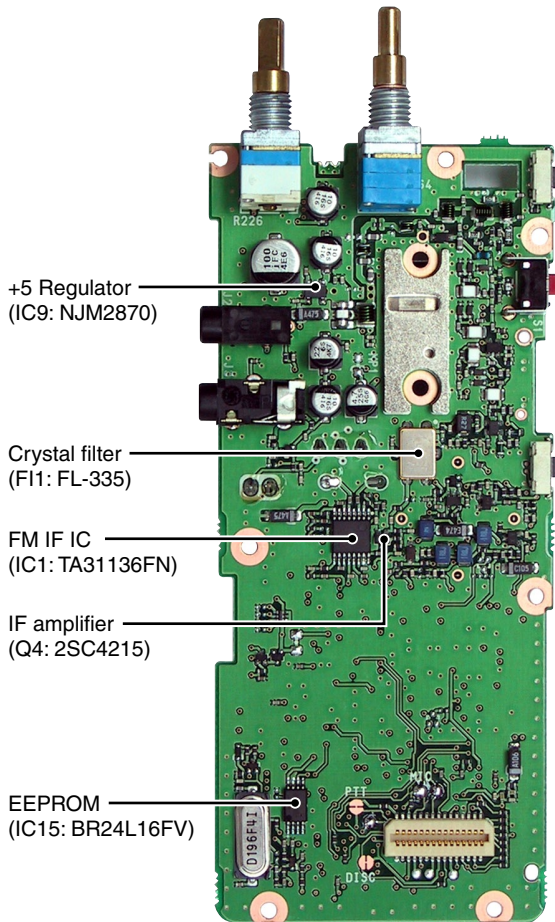
Specifications are measured in accordance with EIA-152-C/204D, TIA-603 or EN 300 086.

All stated specifications are subject to change without notice or obligation.

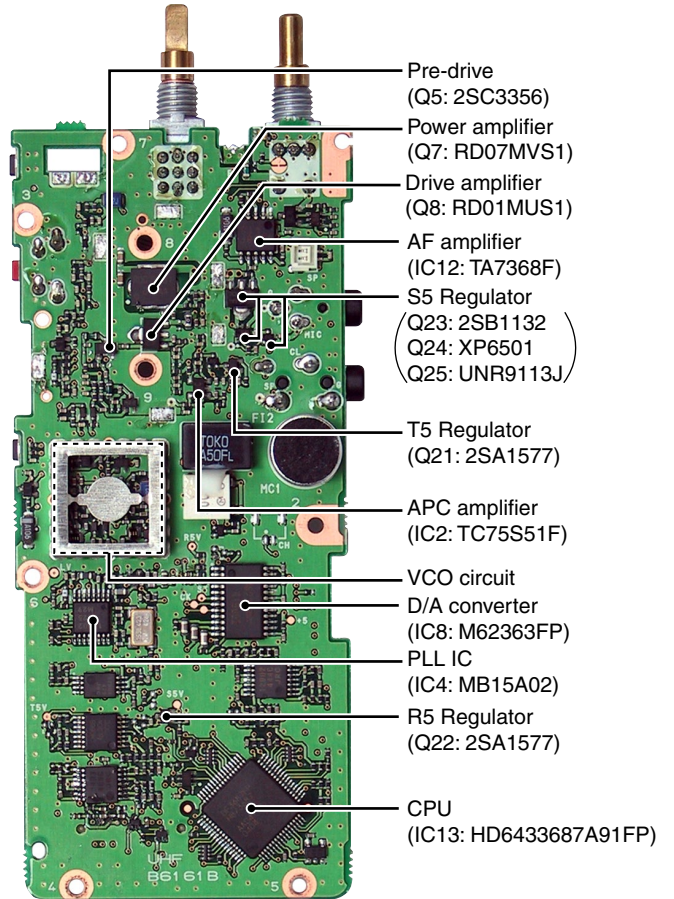
SECTION 2 INSIDE VIEWS

• MAIN UNIT

TOP VIEW



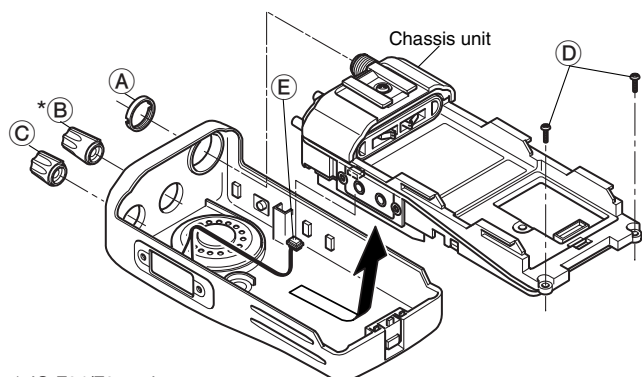
BOTTOM VIEW



SECTION 3 DISASSEMBLY INSTRUCTIONS

● REMOVING THE CHASSIS UNIT

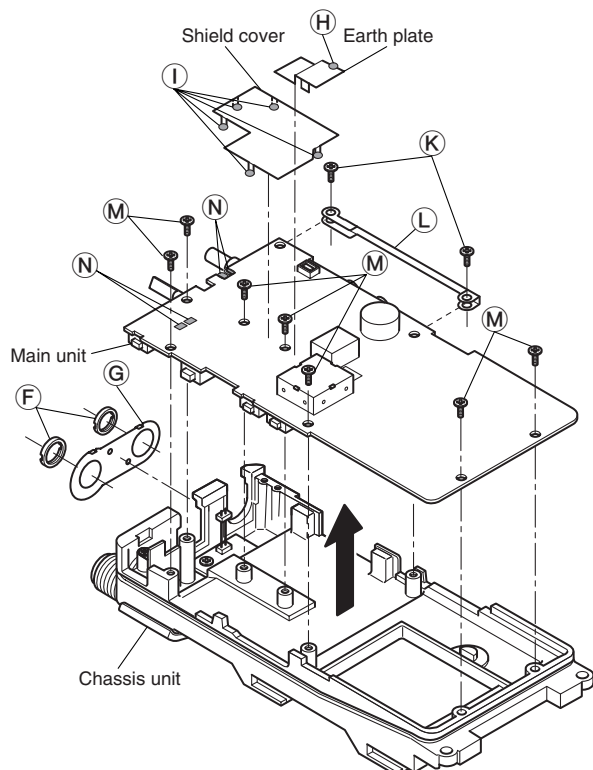
- ① Unscrew 1 nut (A), and remove 2 knobs * (B), (C).
- ② Unscrew 2 screws (D).
- ③ Take off the chassis unit in the direction of the arrow.
- ④ Unplug the connector (E) from the chassis unit.



*: IC-F24/F25 only

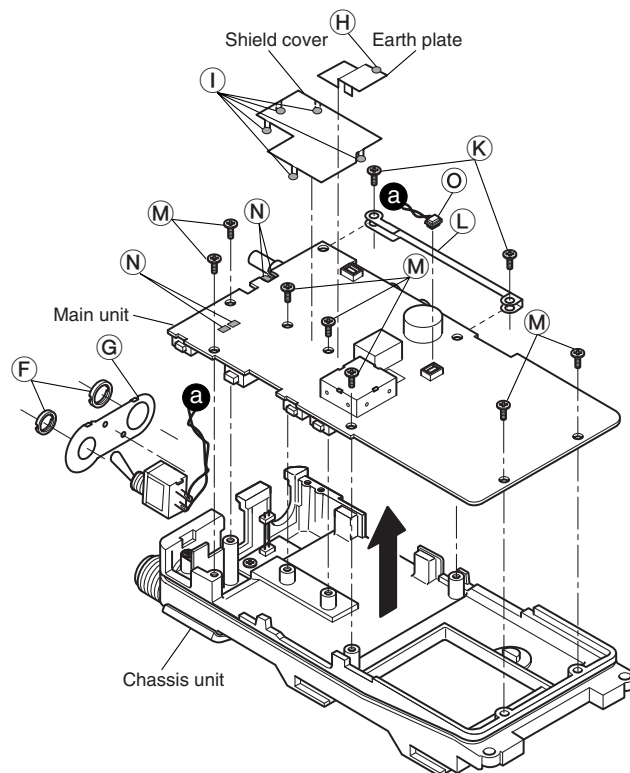
● REMOVING THE MAIN UNIT (IC-F24/F25)

- ① Unscrew 2 nuts (F), and remove the top plate (G).
- ② Unsolder 1 point (H), and remove the earth plate.
- ③ Unsolder 5 points (I), and remove the shield cover.
- ④ Unscrew 2 screws (K), and remove the side plate (L).
- ⑤ Unscrew 7 screws (M).
- ⑥ Unsolder 4 points (N), and take off the main unit in the direction of the arrow.



● REMOVING THE MAIN UNIT (IC-F24S/F25S)

- ① Remove the switch connector (O).
- ② Unsolder 2 nuts (F), and remove the top plate (G).
- ③ Unsolder 1 point (H), and remove the earth plate.
- ④ Unsolder 5 points (J), and remove the shield cover.
- ⑤ Unscrew 2 screws (K), and remove the side plate (L).
- ⑥ Unscrew 7 screws (M).
- ⑦ Unsolder 4 points (N), and take off the main unit in the direction of the arrow.



SECTION 4

CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals enter the antenna connector (CHASSIS; J1) and pass through the low-pass filter (L1, L2, L45, C1–C6, C175). The filtered signals are passed through the $\frac{1}{4}\lambda$ type antenna switching circuit (D2, D5, L5) and then applied to the RF circuit.

4-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the bandpass filter (D3, D4, D7, D8, L7, L8, C21, C23, C24). The filtered signals are amplified at the RF amplifier (Q2) and then passed through the another bandpass filter (D9, D10, C39, C40, C45) to suppress unwanted signals. The filtered signals are applied to the 1st mixer circuit.

D3, D4, D7–D10 employ varactor diodes, that are controlled by the CPU via the D/A converter (IC8), to track the bandpass filter. These varactor diodes tune the center frequency of an RF passband for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal into fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only the desired frequency passes through a crystal filter at the next stage of the 1st mixer.

The RF signals from the bandpass filter are mixed with the 1st LO signals, where come from the RX VCO circuit via the BPF (L12, L38, C49, C304, C305), at the 1st mixer circuit (Q3) to produce a 46.35 MHz 1st IF signal. The 1st IF signal is passed through a monolithic filter (F11) in order to obtain selection capability and to pass only the desired signal. The filtered signal is applied to the 2nd IF circuit after being amplified at the 1st IF amplifier (Q4).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. The double-conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

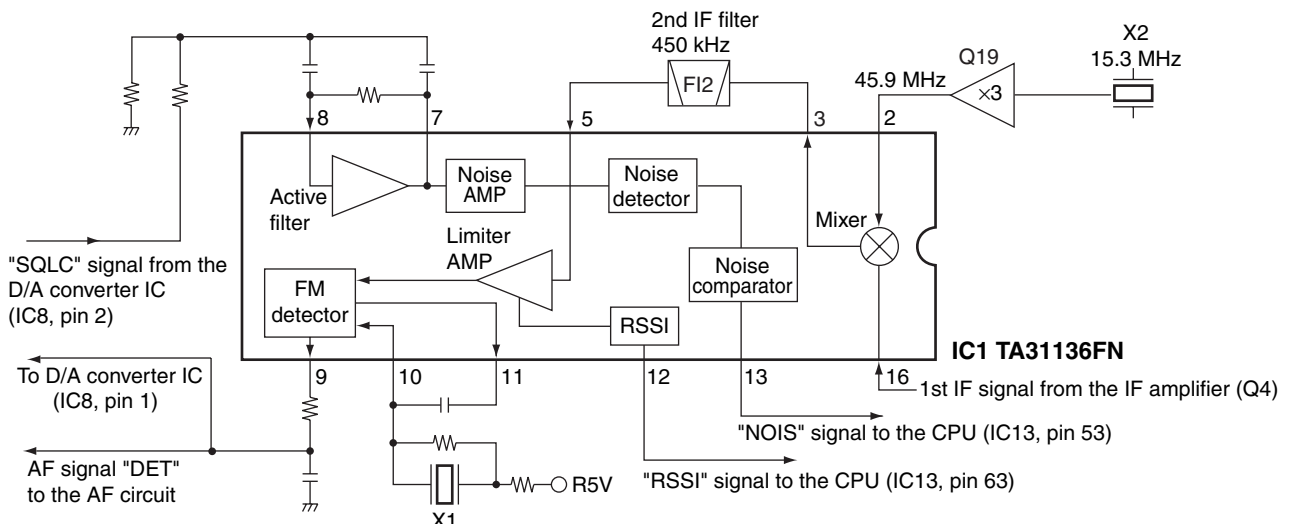
The 1st IF signal from the IF amplifier (Q4) is applied to the 2nd mixer section of the FM IF IC (IC1, pin 16), and is mixed with the 2nd LO signal to be converted into a 450 kHz 2nd IF signal.

The FM IF IC (IC1) contains the 2nd mixer, 2nd local oscillator, limiter amplifier, quadrature detector, active filter and noise amplifier circuits. The 2nd LO signal (45.9 MHz) is produced at the PLL circuit by tripling its reference frequency (15.3 MHz).

The 2nd IF signal from the 2nd mixer (IC1, pin 3) passes through the ceramic filter (F12) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier section (IC1, pin 5) and applied to the quadrature detector section (IC1, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

The demodulated AF signals are output from pin 9 (IC1) as "DET" signal, and are then applied to the AF circuit.

• 2ND IF AND DEMODULATOR CIRCUITS



4-1-5 AF AMPLIFIER CIRCUIT

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

The AF signals from the FM IF IC (IC1, pin 9) pass through the high-pass filter (IC6, pins 3 and 1) to suppress unwanted harmonic components. The signals pass through the RX mute switch (Q34) which is controlled by "RMUT" signal from the CPU (IC13, pin 56), and are then applied to another high-pass filter (IC6, pins 13 and 14). The filtered signals pass through the low-pass filter (IC6, pins 6 and 7) via the analog switch (IC10, pins 1 and 2). The signals are applied to the analog switch (IC10, pin 10) again, and are then applied to the AF power amplifier (IC12, pin 4) via the AF volume (R226). The amplified AF signals are output from pin 10, and are then applied to the internal speaker which is connected to J1 via the [SP] jack (J3).

4-1-6 RECEIVE MUTE CIRCUITS

• NOISE SQUELCH

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some noise components in the AF signals from the FM IF IC (IC1, pin 9) are applied to the D/A converter (IC8, pin 1) as "DET" signal, and are then output from pin 2. The signals are applied to the active filter section in the FM IF IC (IC1, pin 8). The active filter section filters and amplifies noise components. The amplified signals are converted into the pulse-type signals at the noise detector section and output from pin 13 as "NOIS" signal.

The "NOIS" signal from the FM IF IC is applied to the CPU (IC13, pin 53). Then the CPU analyzes the noise condition and outputs the AF mute control signal from the CPU (pin 56) as "RMUT" signal from pin 56. The signal is applied to the RX mute switch (Q34) to control the AF signal muting.

• CTCSS AND DTCS

The tone squelch circuit detects tone signals and opens the squelch only when the receiving signal contains matched subaudible tone (CTCSS or DTCS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the "DET" signals from the FM IF IC (IC1, pin 9) passes through the low-pass filter (IC7, pins 5 and 7) to remove AF (voice) signals, and are then applied to the amplifier (IC7, pin 3). The amplified signals are applied to the CTCSS or DTCS decoder inside of the CPU (IC13, pin 60) as the "CDEC" signal. The CPU outputs AF mute control signal from pin 56, and is then applied to the RX mute switch (Q34) and analog switch (IC10, pins 12 and 13) to control AF signals muting as "RMUT" signal.

4-2 TRANSMITTER CIRCUITS

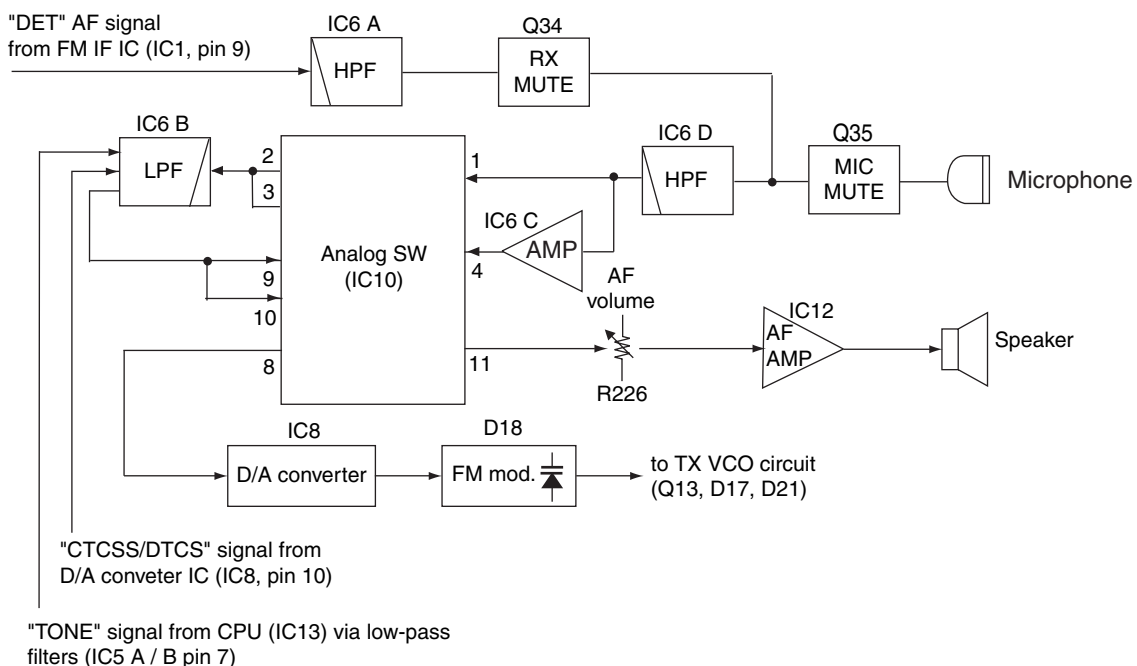
4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals within +6 dB/octave pre-emphasis characteristics from the microphone to a level needed for the modulation circuit.

The AF signals from the microphone are passed through the microphone mute switch (Q35), and are then applied to the amplifier (IC6, pins 9 and 8) via the high-pass filter (IC6, pins 13 and 14). The amplified signals are applied to the analog switch (IC10, pin 4), and outputs from pin 3. The signals pass through the low-pass filter (IC6, pins 6 and 7), then applied to the analog switch (IC10, pin 9) again and output from pin 8.

The signals are applied to the D/A converter (IC8, pin 4). The converted signals output from pin 3, and applied to the modulation circuit (D18) as "MOD" signal.

• ANALOG SWITCHING CIRCUITS



4-2-2 MODULATION CIRCUITS

The modulation circuit modulates the VCO oscillating signal (RF signal) using the audio signals from the microphone.

The AF signals from the D/A converter (IC8, pin 3) change the reactance of varactor diode (D18) to modulate the oscillated signal at the TX VCO circuit (Q13, D17, D21). The modulated VCO signal is amplified at the buffer amplifiers (Q10, Q12) and then applied to the drive amplifier circuit via the T/R switch (D14).

The CTCSS/DTCS signals ("CENC0," "CENC1," "CENC2") from the CPU (IC13, pins 23–25) pass through the low-pass filter (IC5, pins 12 and 14) via 3 registers (R191–R193) to change its waveform. Then the signals are applied to the D/A converter (IC8, pin 9). The output signals from the D/A converter (IC8, pin 10) pass through the low-pass filter (IC6, pins 6 and 7) to be mixed with "MOD" signal, and then applied to the D/A converter again (IC8, pin 4) after passing through the analog switch (IC10, pins 8 and 9).

4-2-3 TRANSMIT AMPLIFIER CIRCUITS

Transmit amplifiers amplify the TX VCO oscillating signal to transmit power level.

The modulated RF signal from the TX VCO circuit passes through the T/R switch (D14) and is amplified at the YGR (Q9), pre-drive (Q5), drive (Q8), and power (Q7) amplifiers to obtain 4 W (max.) of RF power (at 7.2 V DC).

The amplified signal passes through the low-pass filter (L4, C11, C13, C16), antenna switch (D2), the low-pass filter (L1–L3, C2–C5, C175, C176) and power detector (D1, D30), then applied to the antenna connector (CHASSIS unit; J1).

4-2-4 APC CIRCUITS

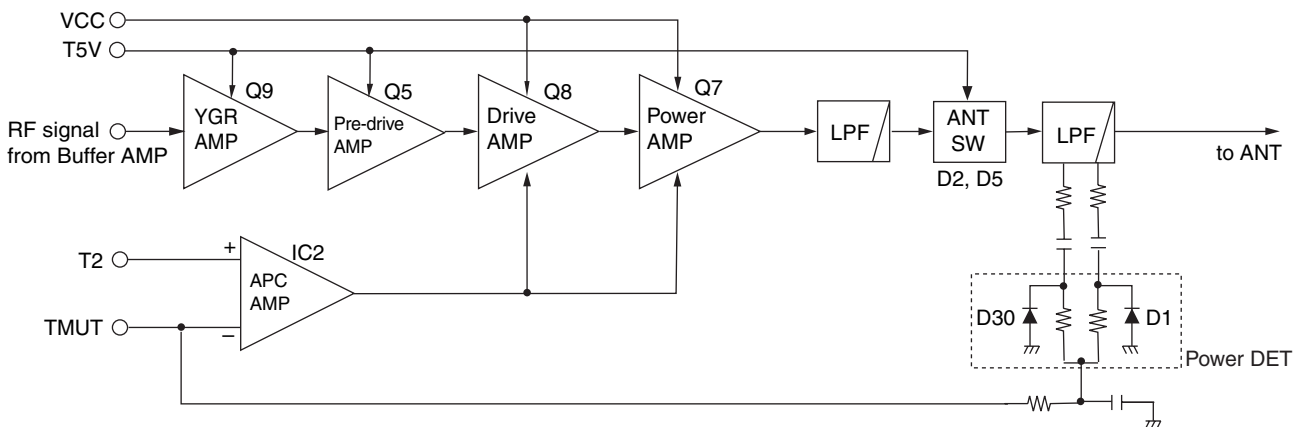
The bias current of the drive (Q8) and power (Q7) amplifiers are controlled by the APC circuit.

The APC circuit (IC2, D1, D30) protects drive and power amplifiers from the reflected signal, and selects output power of HIGH, LOW2 or LOW1.

The power detector (D1, D30) detects transmit output power and converts it into DC voltage. The DC voltage is at a minimum level when the antenna impedance is matched to 50 Ω, and increased when mismatched.

The detected voltage is applied to the differential amplifier (IC2, pin 3), and the "T2" signal from the D/A converter (IC8, pin 23), controlled by the CPU (IC13), is applied to pin 1 for reference. When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the differential amplifier (IC2, pin 4) controls the input current of the drive (Q8), and power (Q7) amplifiers to reduce the output power.

• APC CIRCUITS



4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT

A PLL circuit provides stable oscillation for the transmit frequency and the receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the TX/RX VCO circuits (TX: Q13, D17, D21; RX: Q14, D16, D22). The oscillated signal is amplified at the buffer amplifiers (Q11, Q12) and then applied to the PLL IC (IC4, pin 8) after being passed through the low-pass filter (L32, C206, C208).

The PLL IC (IC4) contains a prescaler, programmable counter, programmable divider and phase detector, charge pump, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency. The phase detected signal is applied to the charge pump to be converted into the DC voltage, and output from pin 5. After passes through the loop filter (C130, C138, C146, C147, R95–R97), the DC voltage is applied to the TX/RX VCO as the lock voltage.

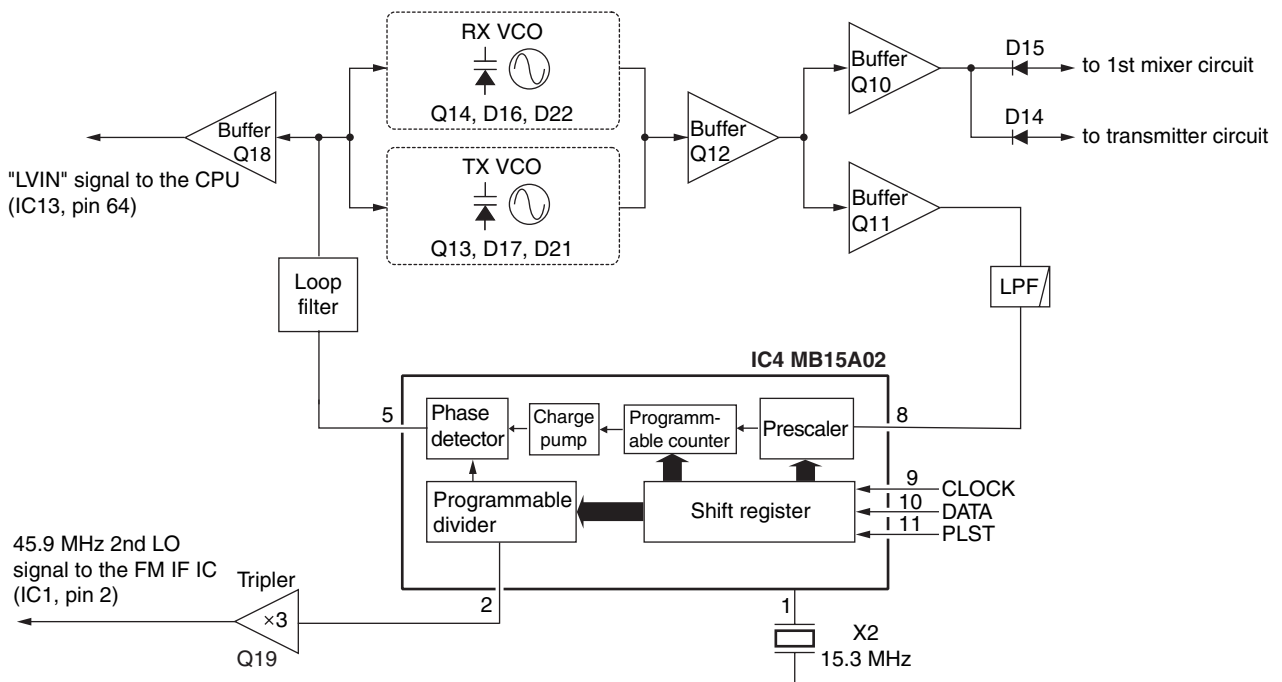
If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

4-3-2 VCO CIRCUITS

The VCO circuit contains a separate RX VCO (Q14, D16, D22) and TX VCO (Q13, D17, D21). The oscillated signal is amplified at the buffer amplifiers (Q10, Q12) and is then applied to the T/R switch (D14 for TX, D15 for RX). Then the receive 1st LO (RX) signal is applied to the 1st mixer circuit (Q3) and the transmit (TX) signal to the pre-drive amplifier (Q9).

A portion of the signal from the buffer amplifier (Q12) is fed back to the PLL IC (IC4, pin 8) via the buffer amplifier (Q11) and low-pass filter (L32, C206, C208) as the comparison signal.

• PLL CIRCUITS



4-4 OTHER CIRCUITS

LED CONTROL CIRCUITS

The LED control circuit is composed of the CPU (IC13), LED driver (Q32) and LED (DS1).

The CPU outputs “RLED” and “TLED” signals from the pins 42 and 43. The signals are applied to the LED driver (Q32, pins 2 and 5). The driver outputs LED control signals to the LEDs (DS1).

CONDITION	COLOR
RECEIVING (2/5-TONE CODE)	ORANGE (Lighting)
LOW BATTERY (Nearly exhausted)	RED (Blinks Slowly)
LOW BATTERY (Almost exhausted)	RED (Blinks Fast)
CLONING	ORANGE (Blinking)
RECEIVING/SQUELCH OPEN	GREEN (Lighting)
TRANSMITTING	RED (Lighting)

4-5 POWER SUPPLY CIRCUIT

VOLTAGE LINE

LINE	DESCRIPTION
VCC	The voltage from the connected battery pack.
+5V	Common 5 V converted from the VCC line at the +5 regulator circuit (IC9). The output voltage is supplied to the D/A converter (IC8), analog SW (IC10), etc.
S5V	Common 5 V converted from the VCC line at the S5 regulator circuit (Q23–Q25). The output voltage is supplied to the ripple filter (Q17), PLL IC (IC4), etc.
R5V	Receive 5 V converted from the S5V line at the R5 regulator circuit (Q22). The output voltage is supplied to the tripler (Q19), FM IF IC (IC1), IF amplifier (Q4), VCO switch (Q15, Q16), 1st mixer (Q3), etc.
T5V	Transmit 5 V converted from the S5V line at the T5 regulator circuit (Q21). The output voltage is supplied to the YGR (Q9), pre-drive (Q5), APC amplifier (IC2), etc.

4-6 PORT ALLOCATION

4-6-1 D/A CONVERTER IC (IC8)

Pin number	Port name	Description
11	BAL	Outputs the modulation balance level control signal. The signal is applied to the reference frequency crystal oscillator (X2, pin 1).
14	LVA	Outputs the PLL lock voltage control signal. The output signal is applied to the RX VCO (Q14, D16, D22) and TX VCO (Q13, D17, D21).
15	REF	Outputs the reference oscillator correcting voltage. The voltage is applied to the reference frequency crystal oscillator (X2, pin 1).
22	T1	Outputs the bandpass filter tuning signal. The output signal is applied to the bandpass filters (D3, D4, D7, D8).
23	T2	<ul style="list-style-type: none"> Outputs the bandpass filter tuning signal during receive. The output signal is applied to the bandpass filters (D9, D10). Outputs the TX power control signal during transmit. The output signal is applied to the APC amplifier (IC2, pin 1).

4-6-2 CPU (IC13)

Pin number	Port name	Description
1	TEMP	Input port for the transceiver's internal temperature detecting signal.
2	BATV	Input port for the detect signal for connecting battery pack's voltage.
7	RES	Input port for power reset signal.
13	SENC0	Output single tone encoder signal.
14	SENC1	
16	DUSE	Outputs DTSC LPF control signal.
18	AFON	Outputs AF power amplifier control signal.
19	SENC2	Output single tone encoder signal.
20	SENC3	
21	CBI0	Input ports for rotary selector.
22	CBI1	
23	CENC0	Output CTCSS/DTCS signals.
24	CENC1	
25	CENC2	
26	CBI2	Input ports for rotary selector.
27	CBI3	
28	SCK	Outputs serial clock signal to the PLL IC (IC4, pin 9), D/A convertor (IC6, pin 7), etc.
29	SO	Outputs serial data to the PLL IC (IC6, pin 8) and D/A convertor (IC6, pin 8).
30	BEEP	Outputs beep audio signals.
31	ESDA	I/O port for data signals from/to the EEPROM (IC15, pin 5).
32	ESCL	Outputs clock signal to the EEPROM (IC15, pin 6).
33	UNLK	Input port for unlock signal from PLL IC.
34	PLST	Outputs strobe signals to the PLL IC (IC4, pin 11).
36	NWC	Output/input port for wide/narrow control signal.
37	DAST	<ul style="list-style-type: none"> • Outputs strobe signals to the D/A convertor (IC8, pin 6). • Input port for the connecting battery type detect signal.
38	S5C	Outputs power save control signal.
39	T5C	Outputs T5 regulator control signal. Low: While transmitting
40	R5C	Outputs R5 regulator control signal. Low: While receiving

Pin number	Port name	Description
42	RLED	Outputs receiving LED control signal.
43	TLED	Outputs transmitting LED control signal.
44	OPT3	I/O ports for option unit.
45	OPT1	
46	OPT2	
47	PTT	Input port for the PTT switch detection signal. Low : While the PTT switch is pushed.
48	SI	Serial Bus inputport.
49	CLI	Input port for the cloning data signal.
50	CLO	Outputs the cloning data signal.
53	NOIS	Input port for the noise signal from the FM IF IC (MAIN unit; IC1, pin 13).
54	CIRQ	Input port for option unit detection.
55	CCS	Outputs chip select signal.
56	TMUT	Outputs transmit mute signal.
57	RMUT	Input port for AF mute signal from the RX circuit.
58	MMUT	Outputs MIC mute signal.
59	REMO	Inputs key signal from remote mic.
60	CDEC	Input port for CTCSS/DTCS signal from the amplifier (IC5, pin 8).
61	SDEC	Input port for single tone decode signal from the LPF (IC5, pin 8).
62	KEY	Inputs key input signal.
63	RSSI	Input port for the S-meter signal from the FM IF IC (IC1, pin 12).
64	LVIN	Input port for the PLL lock voltage.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

When adjusting IC-F24/F25/S, the optional CS-F14 ADJ ADJUSTMENT SOFTWARE (Rev. 1.0 or later), JIG cable (see the illust below) and OPC-478 (RS-232 type) or OPC-478U (USB type) CLONING CABLE are required.

■ REQUIRED TEST EQUIPMENTS

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.2 V DC Current capacity : 5 A or more	Audio generator	Frequency range : 300–3000 Hz Output level : 1–500 mV
FM deviation meter	Frequency range : DC–600 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 20 or 30 dB Capacity : 10 W or more
Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 100–600 MHz Output level : 0.1 μV–32 mV (–127 to –17 dBm) (As open circuit.)
Digital multimeter	Input impedance : 10 MΩ/V DC or better		
RF power meter (terminated type)	Measuring range : 1–10 W Frequency range : 100–600 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
SINAD meter	Measuring range : 20–20 kHz	AC millivoltmeter	Measuring range : 10 mV–10 V

■ SYSTEM REQUIREMENTS

- Microsoft® Windows® 98/SE/ME/2000/XP
- RS232C/USB port

■ BEFORE STARTING SOFTWARE ADJUSTMENT

Clone adjustment frequencies, TX power, CTCSS frequency, DTCS code and IF bandwidth (see ADJUSTMENT CONFIGURATION on the next page) into the transceiver using with the CS-F14 CLONING SOFTWARE before starting SOFTWARE ADJUSTMENTS. Otherwise, the transceiver can not be adjusted.

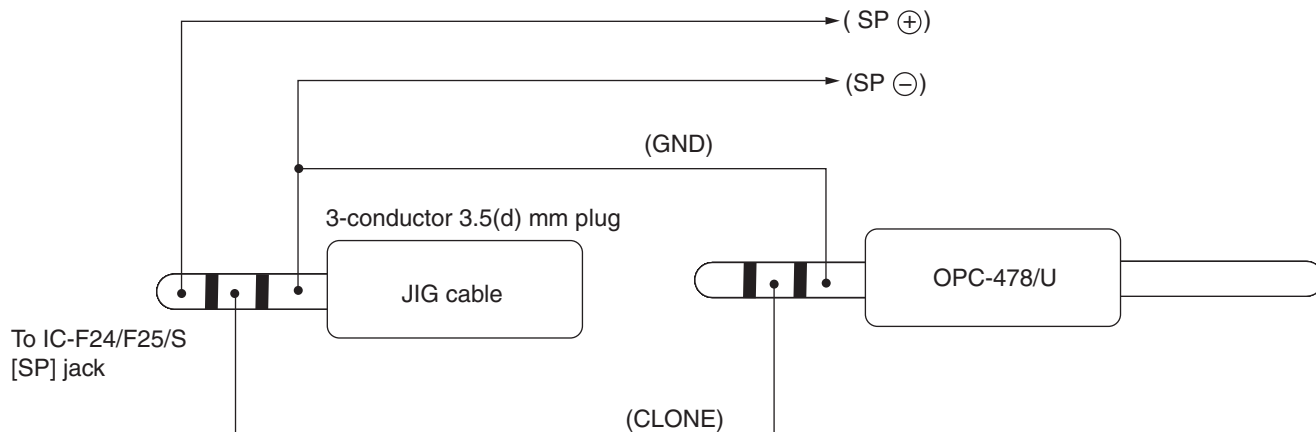
CAUTION!: BACK UP the originally programmed memory data in the transceiver before programming the adjustment frequencies. When program the adjustment frequencies into the transceiver, the transceiver's memory data will be overwritten and lose original memory data at the same time.

■ STARTING SOFTWARE ADJUSTMENT

- (1) Connect IC-F24/F25/S and PC with OPC-478/U and JIG CABLE.
- (2) Turn the transceiver power ON.
- (3) Boot up Windows, and click the program group 'CS-F14 ADJ' in the 'Programs' folder of the [Start] menu, then CS-F14 ADJ's window appears.
- (4) Click 'Connect' on the CS-F14's window, then appears IC-F14's up-to-date condition.
- (5) Set or modify adjustment data as desired.

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• JIG CABLE



5-2 CONFIGURATION LIST FOR ADJUSTMENTS

- IC-F24/F25 -

[US2]=USA-02, [GE2]=GEN-02, [EU2]=EUR-02, [US3]=USA-03, [GE3]=GEN-03

CH.	FREQUENCY (MHz)		SETTING CONDITION	CH.	FREQUENCY (MHz)		SETTING CONDITION
	[US2], [EU2], [GE2]	[US3], [GE3]			[US2], [EU2], [GE2]	[US3], [GE3]	
1	400.000	450.000	Set TX power to High.	7	435.000	485.000	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Wide/Middle. (Middle : EUR only)
2	400.000	450.000	Set TX power to Low1.	8	435.000	485.000	Set TX power to Low1. Set IF bandwidth to Narrow.
3	400.000	450.000	Set TX power to Low2.				
4	435.000	485.000	Set TX power to Low1.				
5	470.000	520.000	Set TX power to Low1.	9	435.000	485.000	Set TX power to Low1. Set IF bandwidth to Wide/Middle. (Middle : EUR only)
6	435.000	485.000	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Narrow.	10	435.000	485.000	Set TX power to Low1. Set IF bandwidth to Wide. Set CTCSS to 151.4Hz.
				11	400.000	450.000	Set IF bandwidth to Wide.

- IC-F24S/F25S -

- Re-clone these settings every time each category is adjusted. (1-8).

1.PLL LOCK VOLTAGE

2.REFERENCE FREQUENCY

CH.	FREQUENCY (MHz)		SETTING CONDITION
	[US2], [EU2], [GE2]	[US3], [GE3]	
1	400.000	450.000	Set TX power to Low1.
2	470.000	520.000	Set TX power to Low1.

3.TX POWER

CH.	FREQUENCY (MHz)		SETTING CONDITION
	[US2], [EU2], [GE2]	[US3], [GE3]	
1	400.000	450.000	Set TX power to High.
2	400.000	450.000	Set TX power to Low2.
3	400.000	450.000	Set TX power to Low1.

4.FM DEVIATION

CH.	FREQUENCY (MHz)		SETTING CONDITION
	[US2], [EU2], [GE2]	[US3], [GE3]	
1	435.000	485.000	Set TX power to Low1. Set IF bandwidth to Narrow.
2	435.00	485.00	Set TX power to Low1. Set IF bandwidth to Wide/Middle. (Middle : [EUR] only)

5.MODULATION BALANCE

CH.	FREQUENCY (MHz)		SETTING CONDITION
	[US2], [EU2], [GE2]	[US3], [GE3]	
1	435.000	485.000	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Narrow.
2	435.000	485.000	Set TX power to Low1. Set DTCS code to 007. Set IF bandwidth to Wide/Middle. (Middle : [EUR] only)

6.CTCSS/DTCS DEVIATION

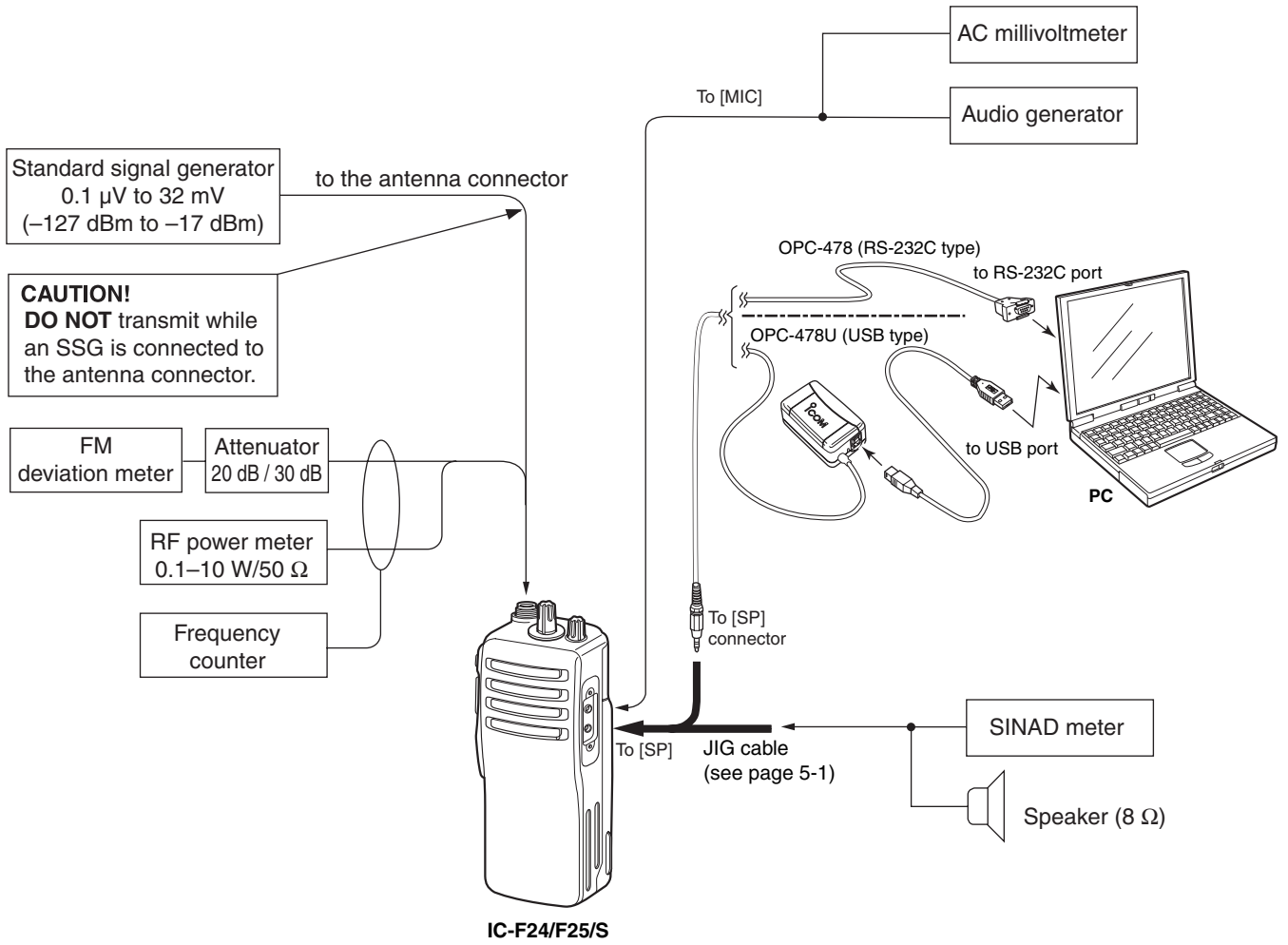
CH.	FREQUENCY (MHz)		SETTING CONDITION
	[US2], [EU2], [GE2]	[US3], [GE3]	
1	435.000	485.000	Set TX power to Low1. Set IF bandwidth to Wide. Set CTCSS to 151.4Hz.

7.RX SENSITIVITY

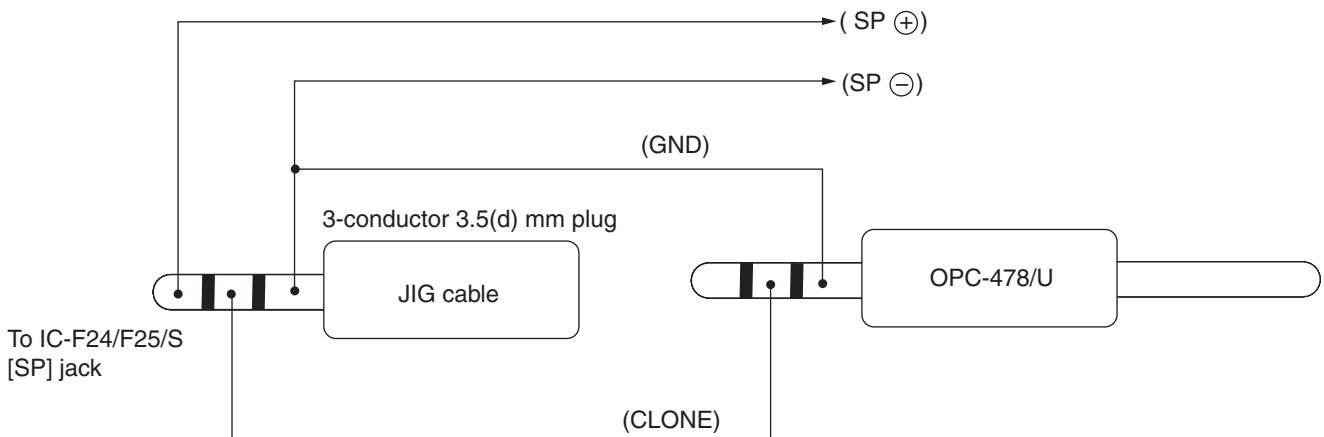
8.SQUELCH LEVEL

CH.	FREQUENCY (MHz)		SETTING CONDITION
	[US2], [EU2], [GE2]	[US3], [GE3]	
1	400.000	450.000	Set IF bandwidth to Wide.

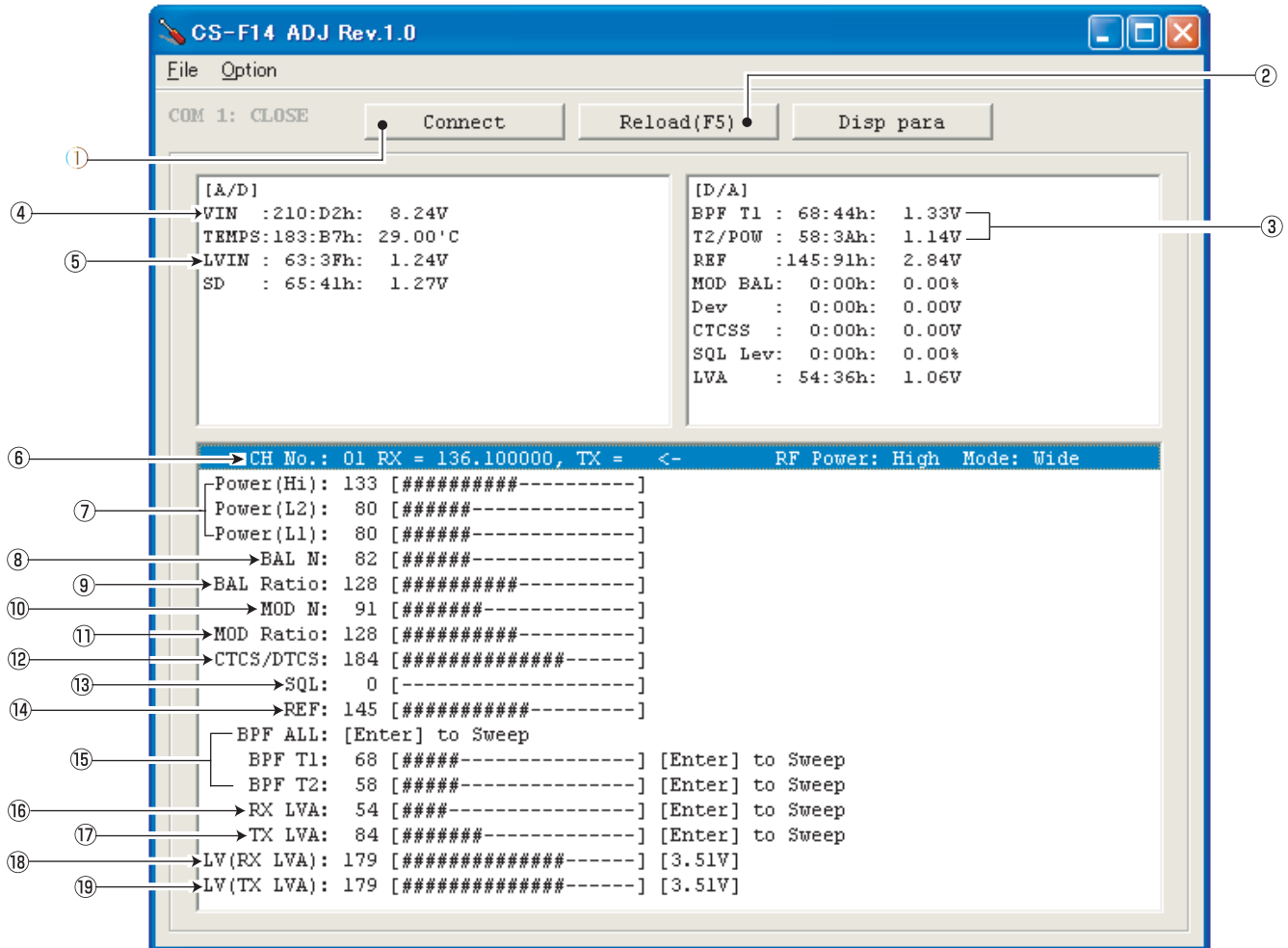
• CONNECTION



• JIG CABLE



• PC SCREEN EXAMPLE

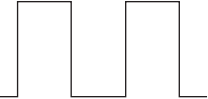


NOTE: The above screen is an example.
Each transceiver has its own specific values for each setting.

- | | |
|-------------------------------------|--|
| ①: Transceiver's connection state | ⑫: CTCSS/DTCS deviation |
| ②: Reload adjustment data | ⑬: Squelch level |
| ③: Receive sensitivity measurement | ⑭: Reference frequency |
| ④: Connected DC voltage measurement | ⑮: Receive sensitivity (automatically) |
| ⑤: PLL lock voltage measurement | ⑯: PLL lock voltage for RX (automatically) |
| ⑥: Operating channel select | ⑰: PLL lock voltage for TX (automatically) |
| ⑦: RF output power | ⑱: PLL lock voltage for RX (manually) |
| ⑧: FM deviation balance (Narrow) | ⑲: PLL lock voltage for RX (manually) |
| ⑨: FM deviation balance (Wide) | |
| ⑩: FM deviation (Narrow) | |
| ⑪: FM deviation (Wide) | |

5-3 SOFTWARE ADJUSTMENTS (TRANSMITTING)

Select the operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	
		UNIT	LOCATION		
PLL LOCK VOLTAGE [LV (RX LVA)] [LV (TX LVA)]	1	<ul style="list-style-type: none"> Operating CH : CH2 (*CH1) Receiving 	PC screen	"LVIN" item on the CS-F14 ADJ's screen.	1.0 V
	2	<ul style="list-style-type: none"> Operating CH : CH2 (*CH1) Connect an RF power meter or 50 Ω dummy load to the antenna connector. Transmitting 			1.0 V
	CONVENIENT: PLL LOCK VOLTAGE can be adjusted automatically. Select "TX LVA"/"TX LVA" item on the CS-F14 ADJ screen, and push [ENTER] key.				
	3	<ul style="list-style-type: none"> Operating CH : CH5 (*CH2) Receiving 	PC screen	"LVIN" item on the CS-F14 ADJ's screen.	3.3–4.5 V (Verify)
	4	<ul style="list-style-type: none"> Operating CH : CH5 (*CH2) Connect an RF power meter or 50 Ω dummy load to the antenna connector. Transmitting 			3.3–4.5 V (Verify)
REFERENCE FREQUENCY [REF]	1	<ul style="list-style-type: none"> Operating CH : CH5 (*CH1) Transmitting 	Top panel	Loosely couple the frequency counter to the antenna connector.	470.0000 MHz [US2], [EU2], [GE2] 520.0000 MHz [US3], [GE3]
OUTPUT POWER [Power (Hi)]	1	<ul style="list-style-type: none"> Operating CH : CH1 (*CH1) Transmitting 	Top panel	Connect the RF power meter to the antenna connector.	4.0 W
[Power (L2)]	2	<ul style="list-style-type: none"> Operating CH : CH3 (*CH2) Transmitting 			2.0 W
[Power (L1)]		<ul style="list-style-type: none"> Operating CH : CH2 (*CH3) Transmitting 			1.0 W
FM DEVIATION [MOD N] (Narrow)	1	<ul style="list-style-type: none"> Operating CH : CH8 (*CH1) Set the deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P_P)/2 Connect the audio generator the [MIC] connector and set as : 1.0 kHz 150mV rms Transmitting 	Top panel	Connect the FM deviation meter to the antenna connector through the attenuator.	±2.10 kHz
[MOD Ratio] (Middle; EUR only)	2	<ul style="list-style-type: none"> Operating CH : CH9 (*CH2) Transmitting 			±3.20 kHz
[MOD Ratio] (Wide)	3	<ul style="list-style-type: none"> Operating CH : CH9 (*CH2) Transmitting 			±4.10 kHz
MODULATION BALANCE [BAL N] (Narrow)	1	<ul style="list-style-type: none"> Operating CH : CH6 (*CH1) No audio applied to the [MIC] input. Set the deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P_P)/2 Transmitting 	Top panel	Connect the FM deviation meter with the oscilloscope to the antenna connector through an attenuator.	Set to square wave form 
[BAL Ratio] (Middle; EUR only)	2	<ul style="list-style-type: none"> Operating CH : CH7 (*CH2) Transmitting 			
[BAL Ratio] (Wide)	3	<ul style="list-style-type: none"> Operating CH : CH7 (*CH2) Transmitting 			

*For F24S/F25S adjustment.

5-3 SOFTWARE ADJUSTMENTS (RECEIVING)

• Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
CTCSS/DTCS DEVIATION [CTCS/DTCS]	1 <ul style="list-style-type: none"> • Operating CH : CH10 (*CH1) • No audio applied to the [MIC] input. • Transmitting 	Top panel	Connect the FM deviation meter to the antenna connector through the attenuator.	±0.68 kHz
RX SENSITIVITY [BPF T1], [BPF T2]	1 <ul style="list-style-type: none"> • Operating CH : CH11 (*CH1) • Connect a standard signal generator to the antenna connector and set as: <ul style="list-style-type: none"> Frequency : 400.000 MHz [US2], [EU2], [GE2] 450.000 MHz [US3], [GE3] Level : +20 dBμ (-87dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving <p>CONVENIENT: RX SENSITIVITY can be adjusted automatically. Select "BPF ALL" item on the CS-F14 ADJ's screen, and push [ENTER] key.</p>	Side Panel	Connect the SINAD meter with an 8 Ω load to the [SP] jack through the JIG cable.	Minimum distortion level
SQUELCH LEVEL [SQL]	1 <ul style="list-style-type: none"> • Operating CH : CH11 (*CH1) • Connect an SSG to the antenna connector and set as: <ul style="list-style-type: none"> Frequency : 400.000 MHz [US2], [EU2], [GE2] 450.000 MHz [US3], [GE3] Level : -14 dBμ (-121dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving 	Side pannel	Connect a speaker to the [SP] jack through the JIG cable.	Set "SQL level" to close squelch. Then set "SQL level" at the point where the audio signals just appears.

*For F24S/F25S adjustment.

[MAIN UNIT]

Table with columns: REF NO., ORDER NO., DESCRIPTION, M., H/V LOCATION. Contains parts list for MAIN UNIT.

[US2S]=F24S USA-02, [GE2S]=F24S GEN-02, [EU2S]=F25S EUR-02 S.=Surface mount [US3S]=F24S USA-03, [GE3S]=F24S GEN-03

[MAIN UNIT]

Table with columns: REF NO., ORDER NO., DESCRIPTION, M., H/V LOCATION. Contains parts list for MAIN UNIT.

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C324	4030017420	S.CER ECJ0EC1H470J	T	85/13.7
C325	4550006250	S.TAN TEESVA 1A 106M8L	T	90.6/17.2
C326	4510006940	S.ELE EEVFC0J101P	B	87.8/8.9
C333	4030017420	S.CER ECJ0EC1H470J	B	76.8/39.9
C335	4030018860	S.CER ECJ0EB0J105K	B	57.2/21.1
C339	4030016930	S.CER ECJ0EB1A104K	B	5.9/17.2
C340	4030016930	S.CER ECJ0EB1A104K	B	9.3/12.5
C341	4030016930	S.CER ECJ0EB1A104K	B	5.9/10.1
C342	4030017630	S.CER ECJ0EC1H120J	B	18.3/4.2
C343	4030017580	S.CER ECJ0EC1H060C	B	5.6/4.2
C344	4030017640	S.CER ECJ0EC1H150J	B	7.6/9.1
C345	4030016930	S.CER ECJ0EB1A104K	B	11/11.2
C346	4030016930	S.CER ECJ0EB1A104K	B	11/10.1
C347	4030016790	S.CER ECJ0EB1C103K	T	8.8/6.5
C348	4030016930	S.CER ECJ0EB1A104K	T	6/10
C349	4030016930	S.CER ECJ0EB1A104K	T	21.3/14.9
C350	4030017460	S.CER ECJ0EB1E102K	T	59.4/43.4
C354	4030017460	S.CER ECJ0EB1E102K	T	14.2/24.4
C355	4030018080	S.CER ECJ0EB1H182K	T	42.9/22.7
C356	4030018910	S.CER C1608 JB 0J 475K-T	T	35.3/20.6
C357	4030017400	S.CER ECJ0EC1H220J	T	79/25.5
J1	6510021900	S.CNR BM02B-ASRS-TF	T	86.6/6.8
J2	6450001680	CNR HSJ1122-010010		
J3	6450002250	CNR HSJ1456-010320		
J4	6510018430	S.CNR AXN330C038P	B	11.8/30.6
J5	6510021900	S.CNR BM02B-ASRS-TF [US2S], [US3S], [EU2S], [GE2S], [GE3S] only	T	50.4/11.7
F1	5210000830	S.FUS ERBFE3R00U	T	98/14.5
DS1	5040002670	S.LED CL-165HR/YG	T	102.8/12.4
MC1	7700002540	MIC SKP-4538		
S1	2260002840	SW SKHLLFA010		
S2	2260002800	S.SW SW-167 (SKQTLAE010)	B	99.4/44.2
S3	2260002800	S.SW SW-167 (SKQTLAE010)	B	60.9/44.2
S4	2250000490	ECR TP70TF5163-15.9F-2775 [US2], [US3], [EU2], [GE2], [GE3] only		
EP1	6910015370	S.BEA ACZ1005Y-102-T	T	57/29.9
EP2	0910057942	PCB B 6161B		
EP3	6910015370	S.BEA ACZ1005Y-102-T	T	34.7/32

[CHASSIS UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
J1	6910015910	CNR ANT CONNECTOR-104		
J2	6910015860	CNR IMSA-6277S-02A-G		
S1	2260002870	SW AS-243-A13 [US2S], [US3S], [EU2S], [GE2S], [GE3S] only		
SP1	2510001060	SP K036NA500-47		
W1	8900009640	CBL OPC-963		
W2	8900009640	CBL OPC-963 [US2S], [US3S], [EU2S], [GE2S], [GE3S] only		

[ANT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
L601	6200008240	S.COL 0.30-0.9-5TL 14N	B	7.2/12.5
C601	4030017600	S.CER ECJ0EC1H080C	B	5.8/15.3
EP601	0910057920	PCB B 6210		

[CONNECT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C501	4030017460	S.CER ECJ0EB1E102K	T	18.3/15.3
C502	4030016930	S.CER ECJ0EB1A104K	T	9.3/15.3
J501	6910016390	CNR IMSA-9230B-1-02Z145-PT1		
EP501	0910057930	PCB B 6160		

S.=Surface mount

SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

7-1 CABINET PARTS

[MAIN UNIT]

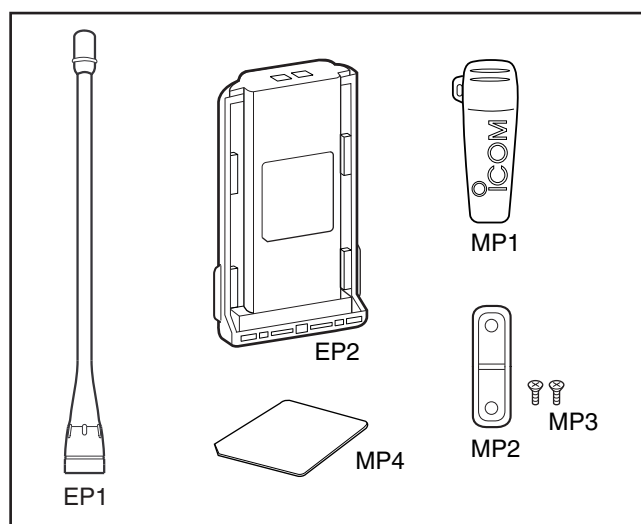
REF.	ORDER. NO.	DESCRIPTION	QTY.
J2	6450001680	HSJ1122010010	1
J3	6450002250	HSJ1456-010320	
R226	7210003061	TP76N00N-15F-A103-2251A	1
S1	2260002840	SKHLLFA010	1
S4	2250000490	TP70TF5163-15.9F-2775 [F24S], [F25S] only	1
MP4	8510016580	2775 shield plate	1
MP5	8510016770	2776 earth plate	1
MC1	7700002540	SKP-4538	1

[ACCESSORIES]

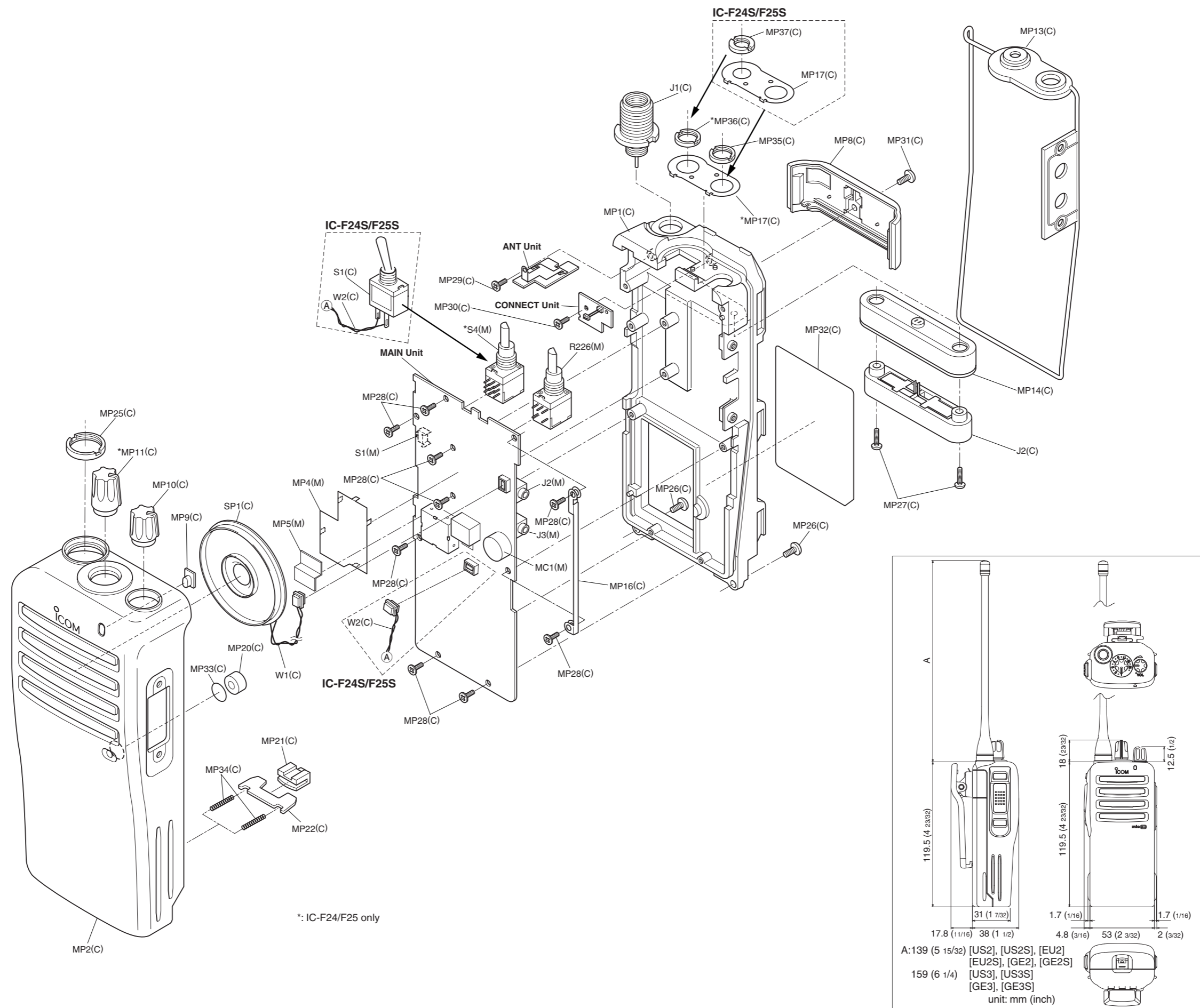
REF.	ORDER. NO.	DESCRIPTION	QTY.
EP1	3310002311	FA-SC25U-1 [US2], [US2S], [EU2] [EU2S], [GE2], [GE2S]	1
	3310002291	FA-SC57U-1 [US3], [US3S] [GE3], [GE3S]	1
EP2	0800007541	BP-231 ACC-1	
MP1	8010019540	MB-94 ACC	1
MP2	8210020560	2721 JACK PANEL	1
MP3	8810004860	Screw M2 x 6 ZK	2
MP4	8930051290	2251 opt sheet	1

[CHASSIS PARTS]

REF.	ORDER. NO.	DESCRIPTION	QTY.
S1	2260002870	AS-243-A13 [F24S], [F25S]only	1
SP1	2510001060	K036NA500-47	1
W1	8900009640	OPC-963	1
W2	8900009640	OPC-963 [F24S], [F25S]only	1
J1	6910015910	Antenna connector-104	1
J2	6910015860	IMSA-6277S-02A-G	1
MP1	8010019690	2775 chassis	1
MP2	8210020920	2775 front panel	1
MP8	8210020550	2721 rear panel	1
MP9	8930063350	2775 lens	1
MP10	8610011930	Knob N-318	1
MP11	8610012130	Knob N-323 [F24], [F25]	1
MP13	8930063330	2775 B-main seal [F24], [F25]	1
	8930063330	2775 A-main seal [F24S], [F25S]	1
MP14	8930063060	2721 terminal rubber	1
MP16	8930063400	2775 side plate	1
MP17	8930063410	2775 B-top plate [F24], [F25]	1
	8930063410	2775 A-top plate [F24S], [F25S]	1
MP20	8930043760	1923 mic seal	1
MP21	8930059360	2600 release button	1
MP22	8930063390	2775 release plate	1
MP25	8830001720	2721 antenna nut	1
MP26	8810009220	Scerw B0 2 x 8 ZK (BT)	2
MP27	8810009560	Scerw M2 x 6 ZK	2
MP28	8810009510	Scerw M2 x 4 NI-ZU (BT)	9
MP29	8810009510	Scerw M2 x 4 NI-ZU (BT)	1
MP30	8810009510	Scerw M2 x 4 NI-ZU (BT)	1
MP31	8810010160	Scerw M3 x 5 SUS ZK	1
MP32	8930051290	2251 opt sheet	1
MP33	8930042350	1922 mic sheet	1
MP34	8930056540	Spring (AH)	2
MP35	8830001700	VR nut (Q)	1
MP36	8830001700	VR nut (Q)	1
MP37	8830001740	VR nut (S) [F24S], [F25S]only	1



Screw abbreviations B0, BT: Self-tapping
 ZK: Black
 SUS: Stainless
 NI-ZU: Nickel-zinc

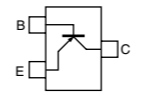
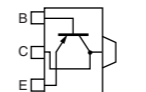
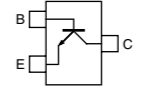
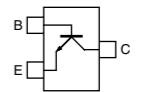
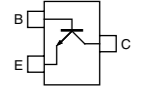
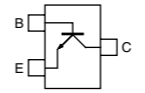
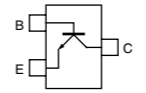
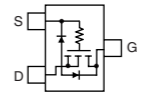
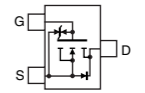
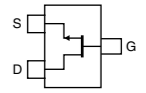
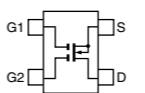
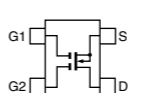
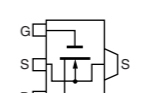
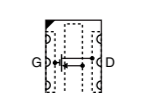
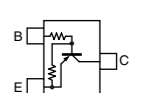
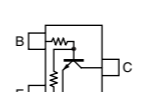
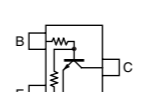
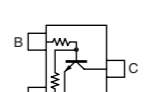
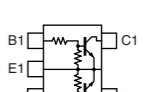
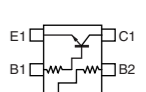
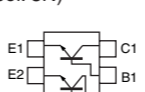


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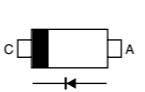
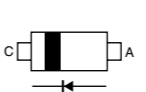
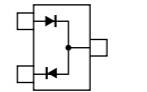
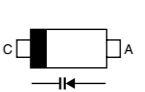
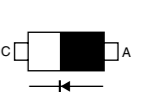
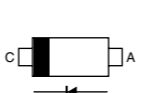
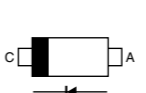
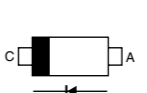
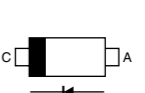
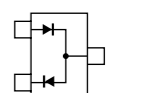
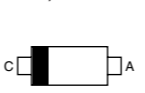
UNIT abbreviation (C): CHASSIS PARTS, (M): MAIN UNIT

SECTION 8 SEMI-CONDUCTOR INFORMATION

• TRANSISTORS AND FETs

2SA2048TL R (Symbol: UL) 	2SB1132 R (Symbol: BARB) 	2SC3356 R25 (Symbol: R25) 	2SC4116 BL (Symbol: LL) 	2SC4215 O (Symbol: QO) 
2SC4226 R25 (Symbol: BR) 	2SC5107 O (Symbol: MFO) 	2SK1829 (Symbol: K1) 	2SK3019 (Symbol: KN) 	2SK880 Y (Symbol: XY) 
3SK293 (Symbol: UF) 	3SK299 U73 (Symbol: U73) 	RD01MUS1 (Symbol: K2) 	RD07MVS1 (Symbol: RD07MVS1) 	UNR9113J (Symbol: 6C) 
UNR911HJ (Symbol: 6P) 	UNR9210J (Symbol: 8L) 	UNR9213J (Symbol: 8C) 	XP1214 (Symbol: 9H) 	XP4216 (Symbol: 8U) 
XP6501 AB (Symbol: 5N) 				

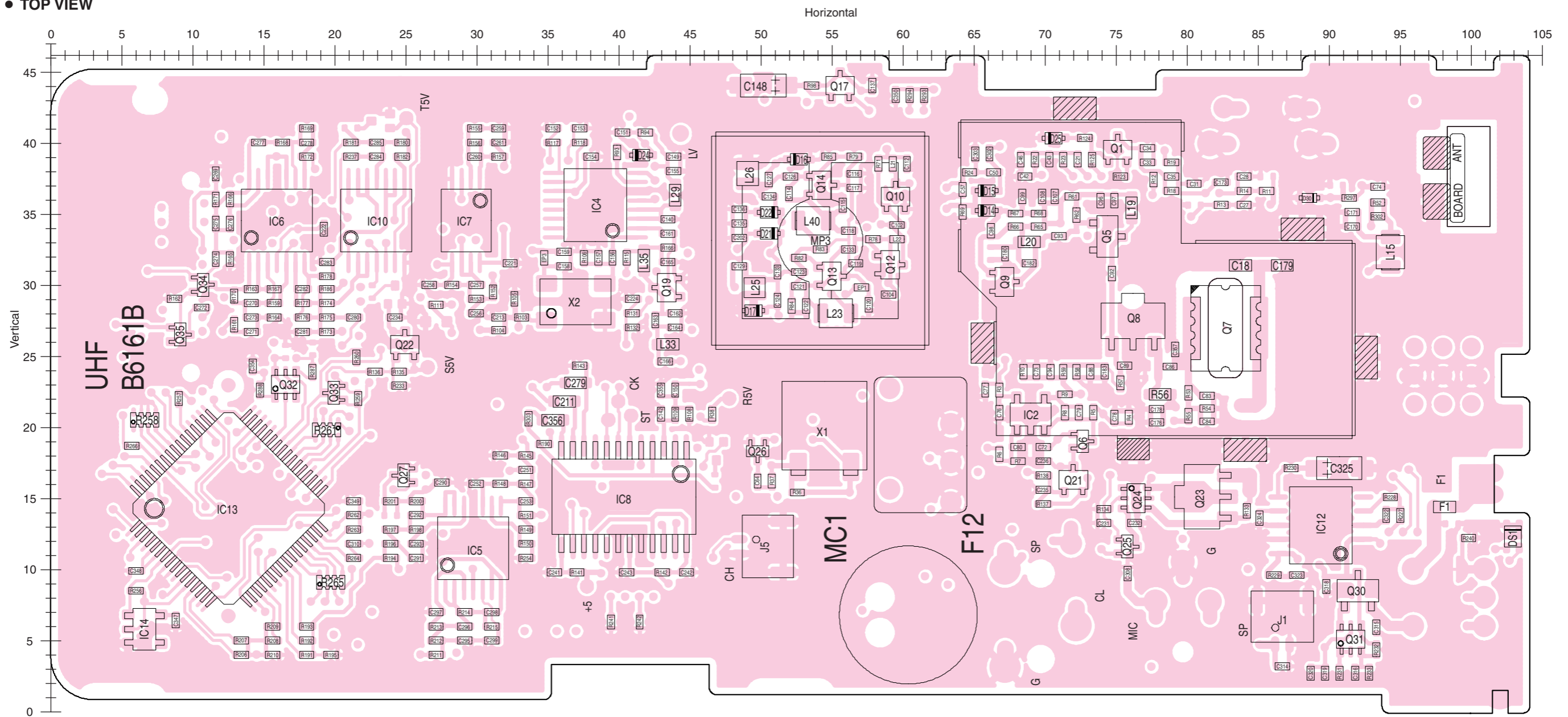
• DIODES

1SS400 (Symbol: A) 	1SV307 (Symbol: TX) 	DAN222 (Symbol: N) 	HVC350B (Symbol: B0) 	MA368 (Symbol: 6L) 
MA8043 L (Symbol: 4_3) 	MA2S077 (Symbol: S) 	MA2S111 (Symbol: A) 	MA2S728 (Symbol: B) 	RB876W TL (Symbol: 3X) 
RB886G (Symbol: C) 				

SECTION 9 BOARD LAYOUTS

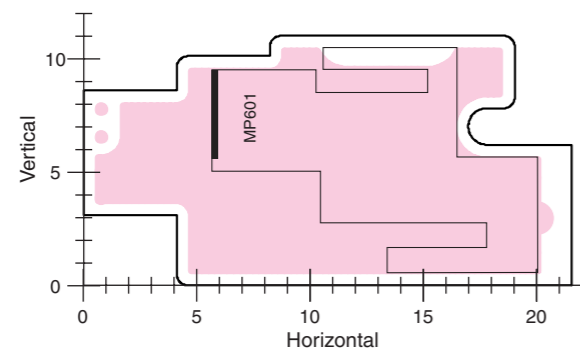
9-1 MAIN UNIT

• TOP VIEW



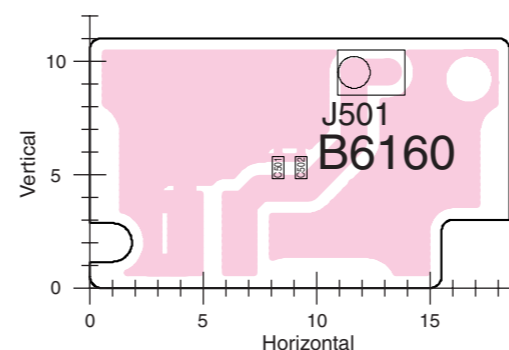
9-2 ANT UNIT

• TOP VIEW

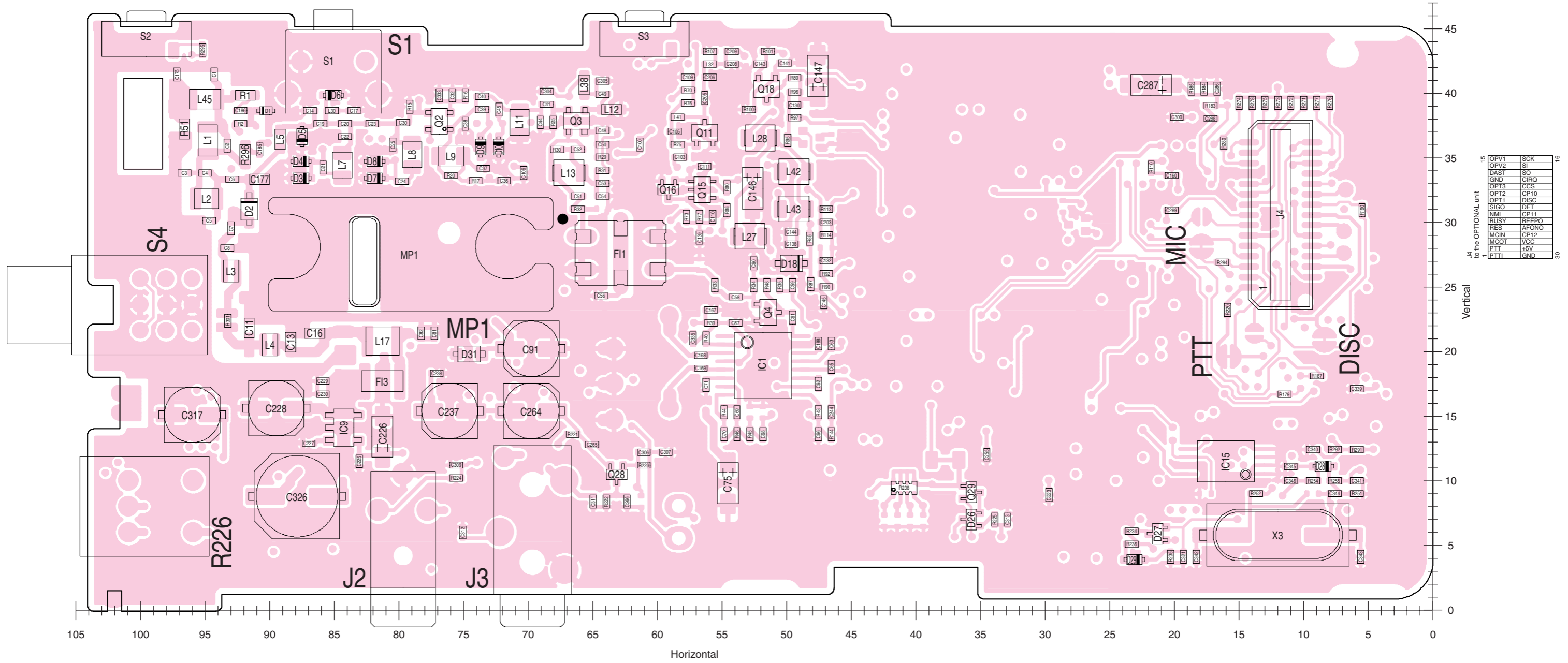


9-3 CONNECT UNIT

• TOP VIEW



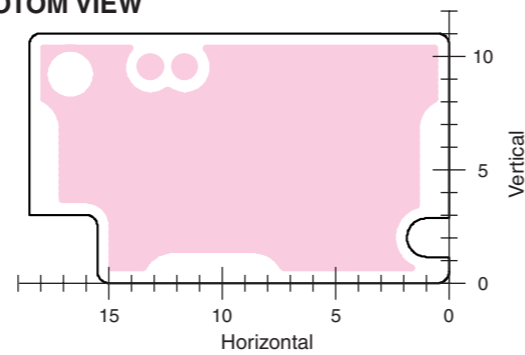
● BOTTOM VIEW



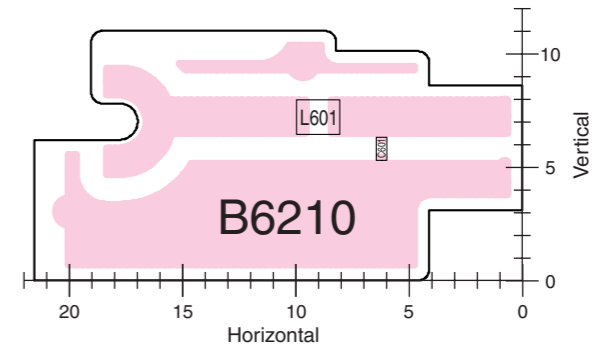
J4 to the OPTIONAL unit

OPV1	SCK
OPV2	SI
DAST	CS
GND	C/R0
OPT3	CCS
OPT2	CP10
OPT1	DISC
SIG0	DET
NMI	CP11
BUSY	BEEPO
RES	AFONO
MCIN	CP12
MCOT	VCC
PTT	HSY
PTTI	GND

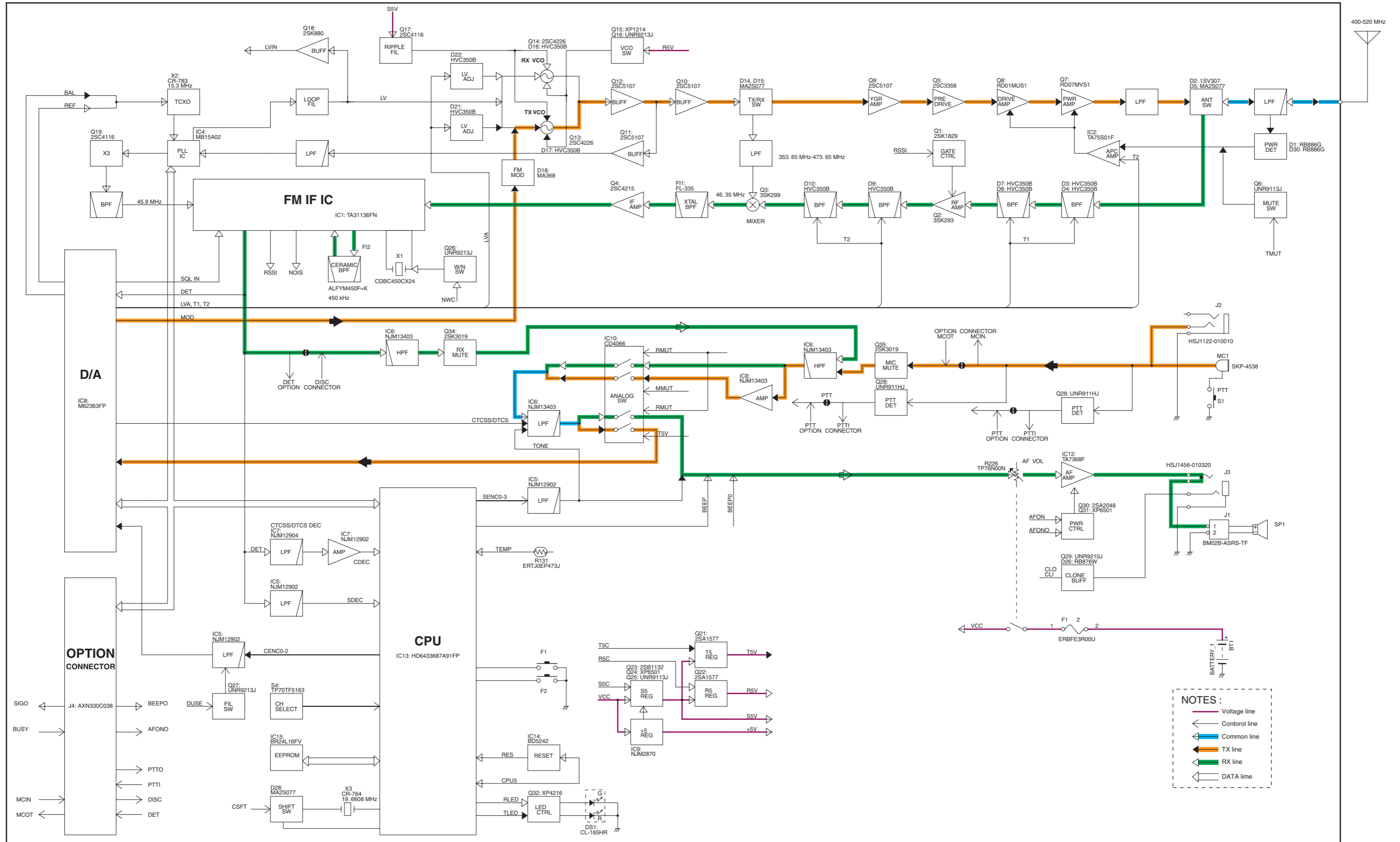
● BOTOM VIEW



● BOTOM VIEW

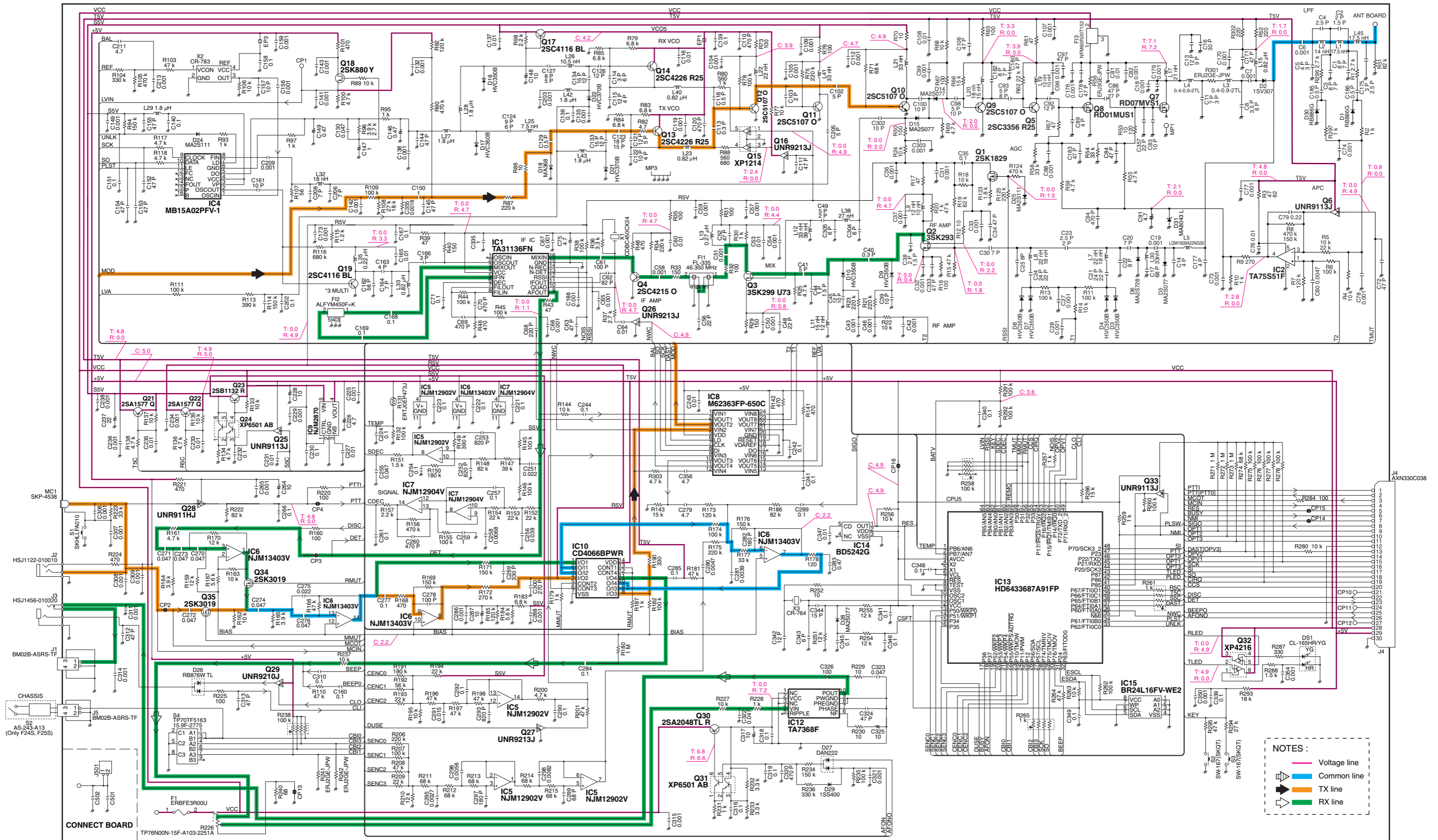


SECTION 10 BLOCK DIAGRAM



SECTION 11 VOLTAGE DIAGRAM

11-1 MAIN UNIT



- NOTES:**
- Voltage line
 - Common line
 - TX line
 - RX line

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